REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1, 9-10, and 15 remain in the application. Claims 1, 9-10, and 15 have been amended. Claims 2-8, 11-14, and 16-17 have been cancelled. Claims 1 and 9-10 have been withdrawn. Rejoinder of claims 1 and 9-10 has been requested.

In item 3 on page 2 of the above-identified Office action, claim 15 has been rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

More specifically, the Examiner has stated that the limitation "using said solder to form a direct chip-substrate connection" is not disclosed in the specification to enable one skilled in the art to make and/or use the invention.

It is noted that the adhesive layer is part of the chip and thus a person skilled in the art does not need to take undue experimentation to make and use a direct chip-substrate

connection by the solder, which basically means that the chip is directly connected the substrate by a solder without any other layer in between. However, the language of claim 15 has been modified to even more clearly define the invention of the instant application.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, first paragraph. Should the Examiner find any further objectionable items, counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided solely for cosmetic and/or clarificatory reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In item 5 on pages 3-4 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over Yamagishi et al. (Japanese Patent Application JP 6-291239) in view of Komata et al. (Japanese Patent Application JP 2-15897), Bacon et al. (US Pat. No. 5,234,153) and Lin (US Pat. No. 4,791,075) under 35 U.S.C. § 103(a).

In item 6 on pages 4-5 of the above-mentioned Office action, claim 15 has been rejected as being unpatentable over

Yamagishi et al. in view of Ishii (Japanese Patent Application JP 6-326210), Bacon et al. and Lin under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references. However, the language of claim 15 has been slightly modified in an effort to overcome the rejection under 35 USC 112, first paragraph, as discussed above, and to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

> said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder.

As already discussed in previous responses, Yamagishi et al. do not disclose a chip-substrate connection by a solder. As can be clearly seen in Fig. 1(C) of Yamagishi et al., there is no solder between the chip 4 and the substrate 1. Rather, a solder is only applied between the housing 5 and the substrate 1 and between the pin bearing pad 3 and the lead pin 2.

The Examiner has stated that Lin discloses in Fig. 2 a semiconductor chip 26 having a rear side and an adhesive 28 and being secured to a substrate 12 using a solder 28 to form a chip-substrate connection (see the first paragraph on page 4 of the Office action). It is noted that the Examiner has used the element referred to by the reference numeral 28 in Lin to refer to both an adhesive layer and a solder according to the invention of the instant application.

Ishii discloses a sub-mount interposed between a laser chip 1 and a metal block 5. As can be seen from Fig. 2 of Ishii, the chip 1 and the substrate 10 do not form a chip-substrate connection by a solder. Rather, there is a barrier layer 7a between the chip 1 and the substrate 10.

Clearly, none of the cited references shows "said semiconductor chip being secured at said rear side to said substrate by one of alloying and brazing using said solder to form a chip-substrate connection by said solder," as recited in claim 15 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art.

Method claim 1 has been amended to correspond to product claim 15 and method claims 9-10 are dependent on claim 1. Rejoinder of method claims 1 and 9-10 is requested upon allowance of product claim 15 under MPEP 821.04.

In view of the foregoing, reconsideration and allowance of claims 1, 9-10, and 15 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants
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